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NOISE MARGIN AWARE POWER EFFICIENT 12T SRAM CELL WITH A HIGH READ AND WRITE ABILITY

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ABSTRACT:
SRAM stability is a major concern in nanometer CMOS technologies. As the most important metrics of SRAM static stability, the static characteristics of SRAM are derived by static characteristic curves (read butterfly curve, standby butterfly curve, read N curve, write N curve and WNM curve). A non-destructive column-selection-enabled 10T SRAM for aggressive power reduction is presented in this brief. It frees a half-selected behaviour by exploiting the bitline-shared data-aware write scheme. The differential-VDD (Diff-VDD) technique is adopted to improve the write ability of the design. In addition, its decoupled read bitlines are given permission to be charged and discharged depending on the stored data bits. In combination with the proposed dropped-VDD biasing, it achieves the significant power reduction. As an enhancement of this project, Reverse Bias Current eliminated, Read-separated, and Write-enhanced SRAM is proposed with 45 nm technology and 12T cells.
Keywords: differential-VDD, non-destructive column-selection, Reverse Bias Current eliminated, dropped-VDD, static characteristic curves.

I. INTRODUCTION:

The analysis of differential-sensing static random-access memory (SRAM) bit cells based on Schmitt-Trigger (ST) for ultralow-voltage operation resolves the basic design conflict between the read and write operations of a traditional 6T bit cell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bit cell. The proposed ST bit cells incorporate a built-in feedback mechanism, achieving process variation tolerance which is a must for future nano scaled technology nodes. A detailed comparison of different bit cells shows that the ST-1, ST-2 and proposed bit cell can operate at lower supply voltages. Portable electronic devices have extremely low power requirement to maximize the battery lifetime. Various device-/circuit-/architectural-level techniques have been implemented to minimize the power consumption [1]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage

power reduces linearly (to the first order) [1]. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors [2], [3]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations.Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write failure, and access-time failure [4]. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [2]. In a given process technology, the maximum supply voltage (referred to as Vmax) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits.Vmax is reducing with the technology scaling due to scaling of gateoxide thickness. The minimum SRAM supply voltage, for a given performance requirement (referred to as Vmin), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, is increasing, and this closes the gap between Vmax and Vmin[5]. Hence, to enable SRAM bit cell operation across a wide voltage range, Vmin has to be further lowered.

II. LITERATURE SURVEY:

NVSRAM is one of the advanced NVRAM technology that is fast replacing the Battery-backed SRAMs that need battery free solutions and long-term retention at SRAM speeds. For instant on-off operation better nonvolatile performance is essential [1]. Better SRAM performance in terms of leakage power, access time, robustness is essential [2].The average power dissipiation should be less [3].The 8T SRAM cell as compared to conventional 6T SRAM cell achieved improved read stability, read current and leakage current [4]. Write power i.e. power dissipiation in SRAM should be less [5]. The issue associated with transistor scaling and power management are addressed [8]. The operating voltage for cell should be minimum [6]. The inverters are optimized for high noise margin[7] The use of SRAM is expected to increase in future for both portable and high performance microprocessor. SRAM plays a critical role in modern microprocessor system, portable devices like PDA, cellular phones, and portable multimedia devices [1]. To achieve higher speed microprocessor, SRAM based cache memories are commonly used. The trend of scaling of device brings several challenges like power dissipation, sub threshold leakage, reverse diode leakage, and stability [2]. Nowadays research on very low threshold voltage and ultra-thin gate oxide are in progressive stage, due to reduction in the threshold voltage and the gate oxide thickness.

III. EXISTING TECHNIQUE:

The original SE-10T SRAM cell of the proposed bitcell is shown in below Fig. A 4T read port composed of an inverter and a transmission gate (TG) is added to the 6T cell, isolating the read path from internal storage nodes. The inverter (M6 and M7) is driven by node QB and drives the read bitline (RBL) through TG (M8 and M9) which is controlled by two complementary read wordlines (WLs). This SE-10T cell can fully charge or discharge RBL by itself during a read operation. Thus, it is totally unnecessary to prepare a precharge circuit for RBL. The dynamic power is consumed on RBL just when the read datum is changed. That is to say, the dynamic power dissipation on RBL is zero if consecutive "0"s or consecutive "1"s are read out. This feature makes it suitable for video processing since image data have the special correlation, and similar data are read out in consecutive cycles [11]. Unfortunately, due to its 6T-like write operation, when initiating a write in a column-selection array, unselected cells in a row (or called half-selected cells) on the selected WL perform dummy read which indicates that the cells just undergo a read behaviour rather than readout during a write operation, thereby experiencing the storage node upset similar to read disturb in the 6T cell. In other words, it is not eligible for the bit-interleaving architecture. In addition, the full rail-to-rail swing occurred on RBL congenitally dissipates more power compared with the differential readout. Meanwhile, bitlines incur more leakage current because of TG. This SE-10T cell has been presented in [11]. However, our propose 10T (thereafter called P-10T) circuit topology is different from the earlier design.

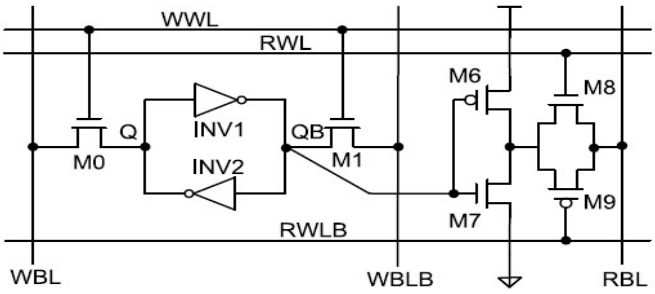

Fig1: Schematic of the SE-10T SRAM cell.

Below Fig. shows the P-10T based on the SE-10T cell. It exhibits improvements in the following aspects compared with the previous circuit. First of all, the bitline-shared data-aware scheme is adopted to enable the column-selection architecture. In Fig, the 6T part of the SE-10T cell is motivated by the *y*-direction (column direction) WL [column WL (CWL)]. In addition, two additional access transistors (M10 and M11) are added to connect the 6T cell, which are activated by the *x*-direction (row direction) write WL (WWL) and at the same time are powered by a complementary write bitline pair (WBL and WBLB). Every extra access transistor and write bitline are shared by two adjacent 10T cells in a row. During a write operation, the data are written into the storage core from shared write bitlines via shared access transistors and internal access transistors, just when row WL and column WL are all switched ON.

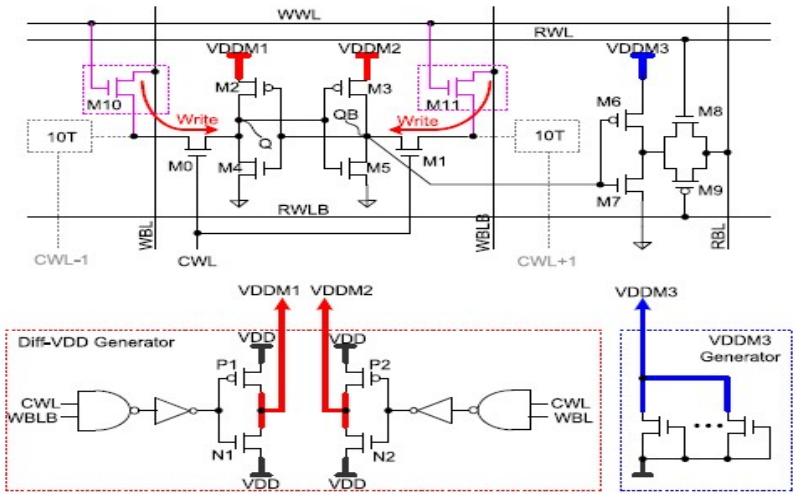

Fig 2: Proposed SE-10T SRAM cell with assistant circuits.

The proposed bit-interleaving-enabled scheme is different from the previous design in [12] where the SRAM array is also able to be column-interleaved by vertical and horizontal WLs. Nonetheless, its write access devices are shared by several bitcells in a column, whereas the write access ones are shared by two bitcells in a row in our design Second, a Diff-VDD strategy is utilized to ameliorate the cell's write ability. We can observe from above Fig. that the power supplies of the 6T cell are coupled to two different virtual power lines (VDDM1 and VDDM2) produced by the Diff-VDD generator. Therein, VDDM1 is generated by ANDing CWL and WBLB to drive a power-ON inverter, in which the source terminals of pMOS and nMOS are all connected to VDD. Similarly, VDDM2 is obtained by ANDing CWL and WBL to drive the other power-ON inverter. These two VDDM lines are dropped differentially according to the values of the required written data. VDDM1 line is dropped at a write access for a "0" datum on WBL (WBLB = 1), while VDDM2 line is inversely dropped for a "1" write access.

Column-Selection-Enabled Array Architecture

To illustrate the column-selection-enabled capability of the proposed design, a matrix of 2 rows by 2 columns (2×2) as an example to describe the elementary write operational principle of the array is shown in below Fig.

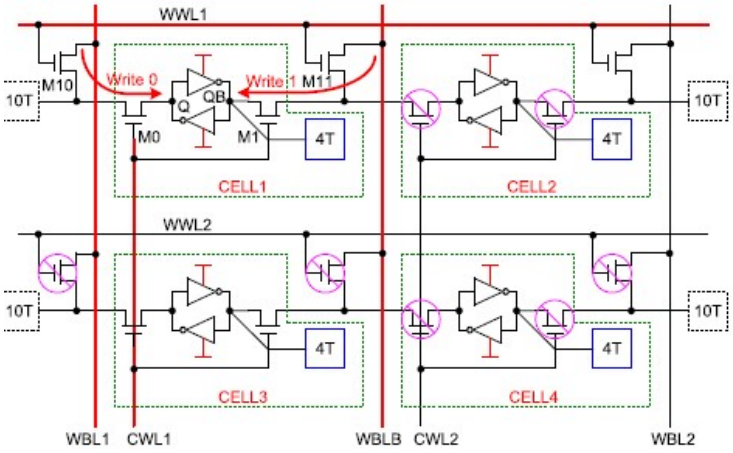

Fig 3: Matrix of 2 × 2 with the proposed bit-interleaving architecture

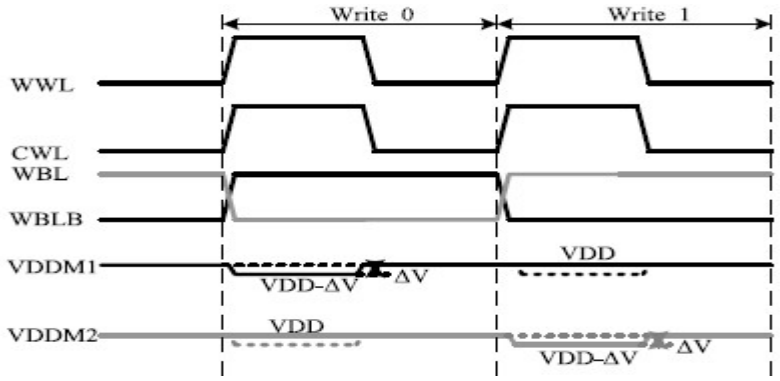

Fig.4 Write waveforms of the P-10T cell.

Suppose the cell1 is chosen for write. The corresponding row WL WWL1 and CWL CWL1 are switched ON, and the matched WBLs (WBL1 and WBLB) are charged or discharged depending on the data. If a "0" is expected to be written into the cell1, WBL1 is pulled down to low, and WBLB resides at high. As a result, storage node *Q* is discharged to "0" by access transistors M0 and M10.

Diff-VDD Write Assist:

The proposed design utilizes the row and column coordination modes of WLs to eliminate the half-selection problem, which leads to the degradation in the write ability due to the series-connected write access nMOSs just like in the Diff-10T cell. This could be highly problematic, particularly in the slow nMOS fast pMOS (SNFP) corner, where the driven strength of nMOS is less than that of pMOS. To solve this issue, the Diff-VDD scheme is presented. Fig. shows the write waveforms of the cell to describe the write assistant circuit how to work Generally, VDDM1 and VDDM2 are all equivalent to VDD because the pMOSs P1 and P2 in the Diff-VDD generator are both turned on (CWL = 0). During a write "0" operation, WLs WWL and CWL are turned on, while bitline WBL is set to low and WBLB goes to high. Subsequently, the nMOS N1 is ON (CWL and WBLB = 1), resulting in a _*V* voltage drop on VDDM1. At this time, VDDM2 resides at VDD since CWL ANDing WBL equals 0.

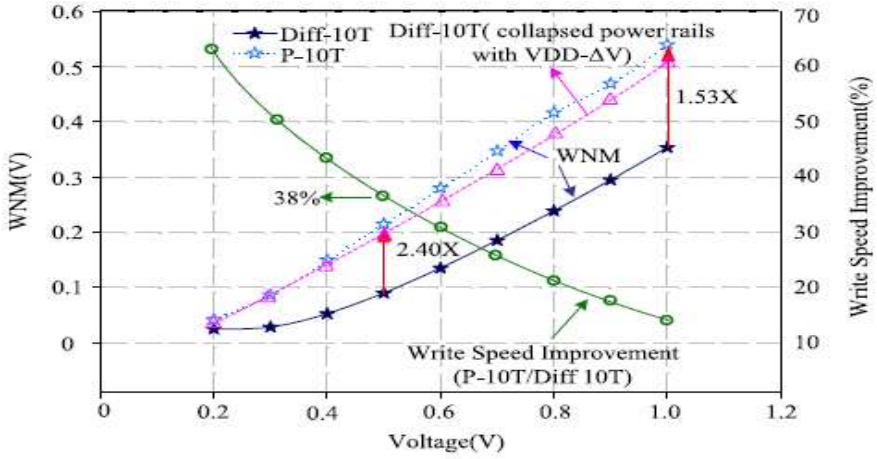

Fig.5 WNM and write speed comparisons between Diff-10T and Diff-10T with collapsed VDD and P-10T. (All the results are simulated in a 65-nm process.)

The dropped VDDM1 is able to attenuate the pullupstrength of pMOS M2 effectively, making the cascaded access nMOSs M0 and M10 absolutely pull the storage node *Q* down to "0." Under the same condition, WBL goes to high, and WBLB is driven to low initiate a write "1" behavior. Similarly, a reduction of _*V* on VDDM2 power rail (CWL and WBL = 1) undermines the pull-up strength of pMOS M3 to ensure that the node QB can be discharged to "0" definitely by M1 and M11.

PROPOSED TECHNIQUE:

REVERSE BIAS CURRENT ELIMINATED, READ-SEPARATED, AND WRITE-ENHANCED TFET 12T BITCELL:

A. Cell structure

The structure of the reverse bias current eliminated, read-separated, and write-enhanced TFET 12T SRAM bitcell is shown in below Fig. The proposed structure consists of two cross-coupled inverters (P1, P2, N1, and N2), and it adopts a read-decoupled access buffer (N7 and N8) to decouple the read current path from the storage node, thereby eliminating read-disturb, avoiding read reverse bias current and enhancing the RSNM. This structure also adopts outward direction access transistors (N3, N4, N5 and N6), and the sources of N5 and N6 are set to the ground at all times. Thus, this structure can effectively avoid reverse bias current in access transistors. As a result, static power consumption can be reduced and the HSNM can be increased.

Single-ended write behavior might affect write delay and power significantly especially for the two access transistors design. However, with two write-assist TFETs, the WSNM can be improved.

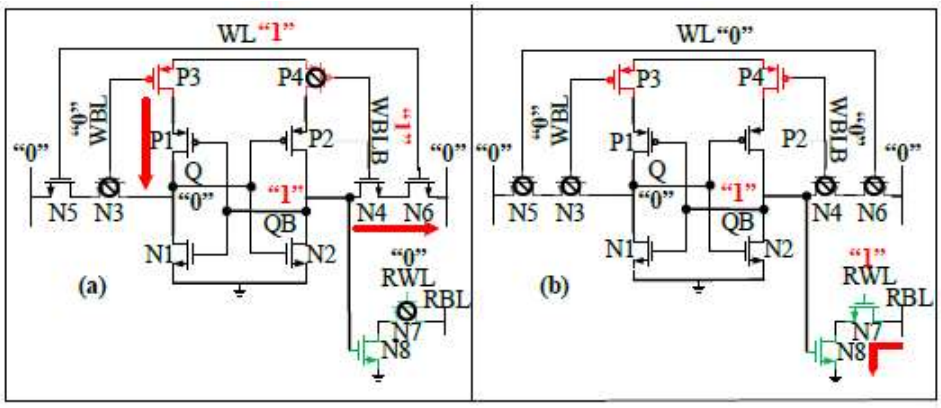

Fig 6: Schematic and current flow paths, (a) the write 1 operation and (b) the read of the proposed 12T SRAM bit cell

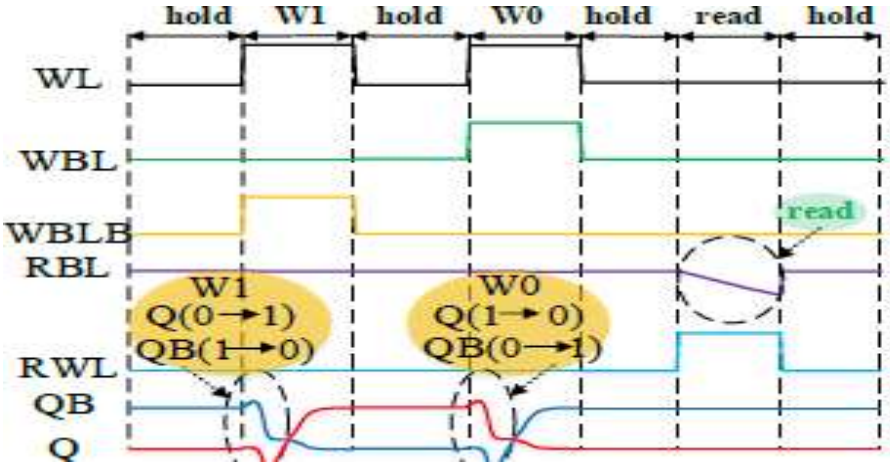

Fig 7: Diagram of the timing, including write, hold, and read.

The source of the pull-up transistor (P1) is connected to the drain of the write-assist transistor (P3), and the source of the pull-up transistor (P2) is connected to the drain of the write-assist transistor (P4). The sources of the write-assist transistors are connected to supply voltage.

B. SRAM operation

In the hold mode, the lines WBL and WBLB are low to turn off the access transistors (N3 and N4) and turn on the write assist transistors (P3 and P4), while the word line (WL) is low to turn off the access transistors (N5 and N6). Therefore, the data can be latched with two cross-coupled inverters.

If the original storage nodes Q and QB store "0" and "1", respectively, the voltage of the storage node QB is pulled to low through the N4 and N6, and the voltage of the storage node Q is pulled to high through the pull-up transistor P1 and write assist transistor P3. Since the write assist transistor P4 is turned off, it is easy to pull the voltage of the storage node QB low. As a result, this cell structure has a strong write 1 ability. Because of the strong write ability, the period of high WBL/WBLB can be very short to ensure that the data of other cells in the same column with the selected cell remain unchanged. The current flow paths in the write 1 operation are depicted in Fig.(a). The principle of writing 0 is similar to that of writing 1. The timing diagram of various signals in different operating modes is shown in above Fig. The waveforms of Q (0→1) and Q (1→0) illustrate the write 1 and write 0 processes, respectively.

As shown in Fig. 3, the read bitline (RBL) is pre-charged to the VDD in advanced in the read operation. Then, the RWL is set to the VDD to turn on N7. If the storage node QB stores "1", the read decision transistor N8 is activated, and the RBL is discharged to the ground through N7 and N8 as depicted in Fig. 2(b). Otherwise, the RBL maintains its pre-charged potential.

1) Hold

In the hold mode, the lines WBL and WBLB are low to turn off the access transistors (N3 and N4) and turn on the write assist transistors (P3 and P4), while the word line (WL) is low to turn off the access transistors (N5 and N6). Therefore, the data can be latched with two cross-coupled inverters.

2) Write

If the original storage nodes Q and QB store “0” and “1”, respectively, the voltage of the storage node QB is pulled to low through the N4 and N6, and the voltage of the storage node Q is pulled to high through the pull-up transistor P1 and write assist transistor P3. Since the write assist transistor P4 is turned off, it is easy to pull the voltage of the storage node QB low. As a result, this cell structure has a strong write 1 ability. Because of the strong write ability, the period of high WBL/WBLB can be very short to ensure that the data of other cells in the same column with the selected cell remain unchanged. The current flow paths in the write 1 operation are depicted in Fig. (a). The principle of writing 0 is similar to that of writing 1. The timing diagram of various signals in different operating modes is shown in Fig. 3. The waveforms of Q (0→1) and Q (1→0) illustrate the write 1 and write 0 processes, respectively.

3) Read

As shown in Fig, the read bitline (RBL) is pre-charged to the VDD in advanced in the read operation. Then, the RWL is set to the VDD to turn on N7. If the storage node QB stores “1”, the read decision transistor N8 is activated, and the RBL is discharged to the ground through N7 and N8 as depicted in Fig. Otherwise, the RBL maintains its pre-charged potential.

IV. RESULTS:

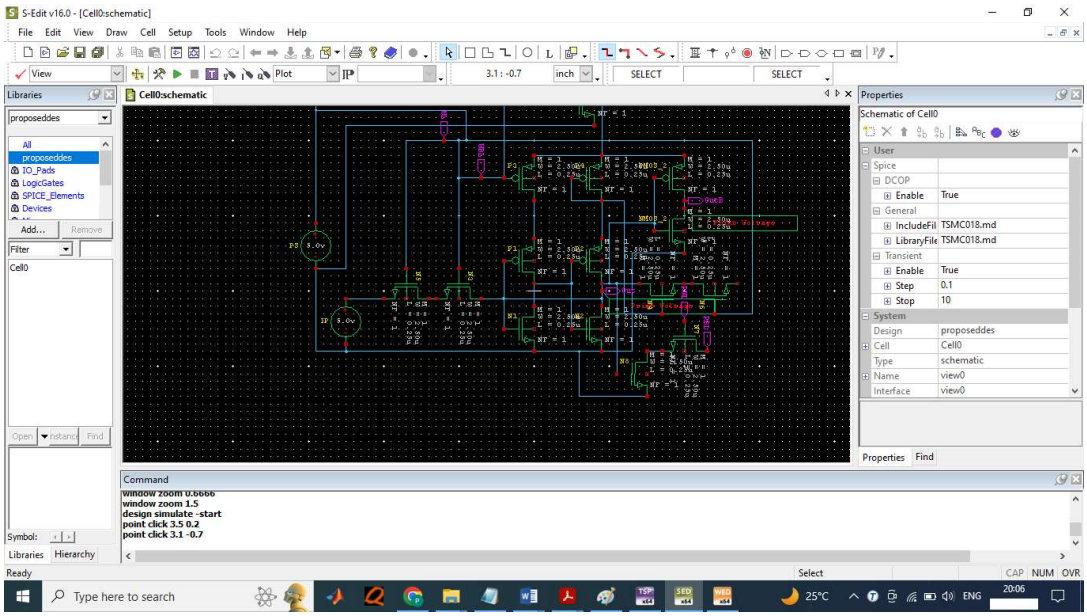

Fig8: Proposed design schematic

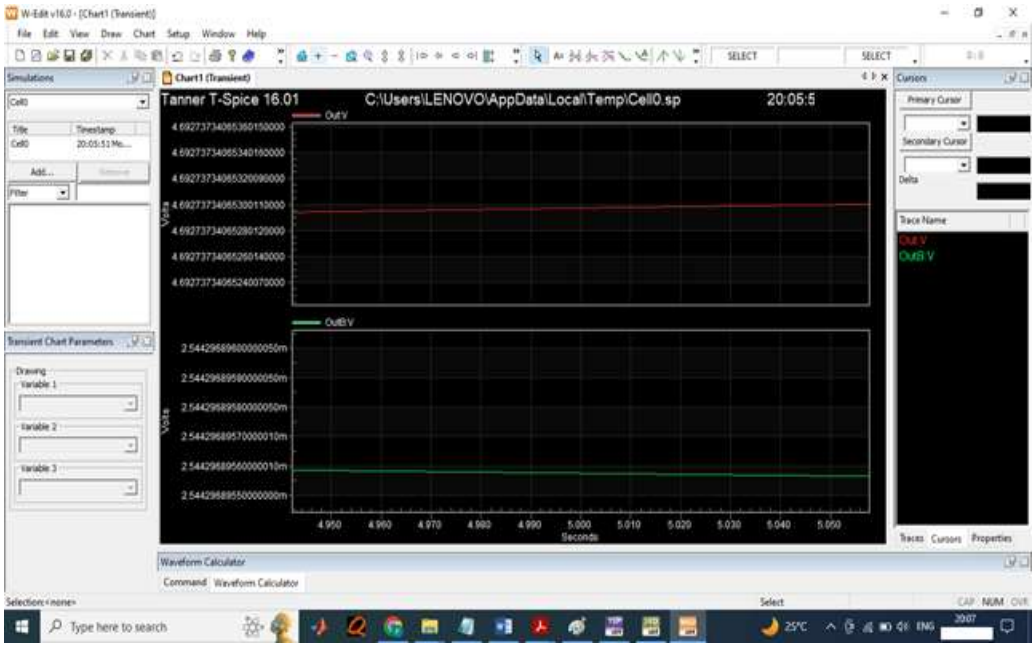

Fig:9 Proposed simulation result

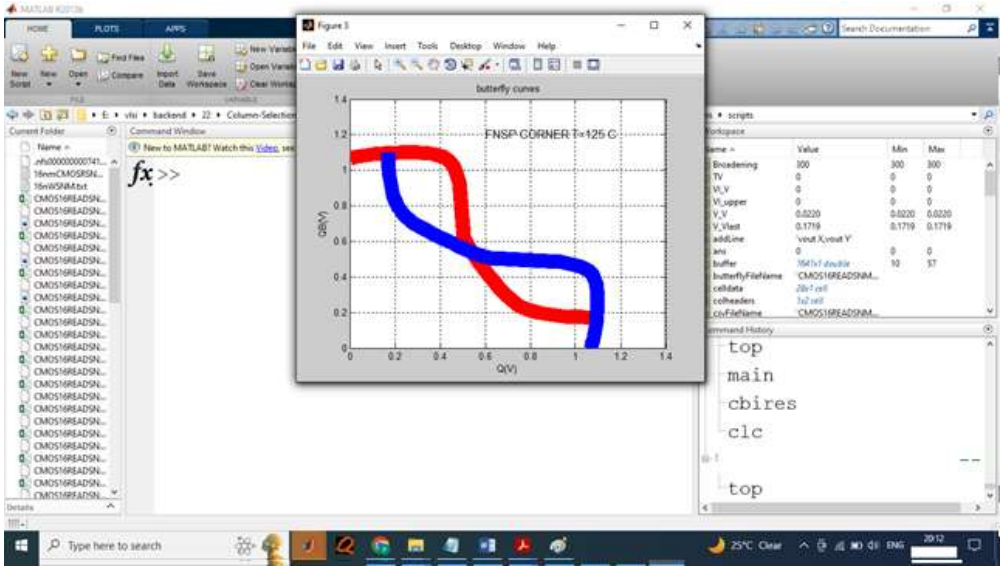

Fig 9: Butterfly curves

V. CONCLUSION AND FUTURE SCOPE:

Finally, an efficient SRAM with proposed technique is implemented, simulated and synthesized with more accurate measurement and calibrations. The different constraints variations against low power CMOS logic families are shortlisted, which shows that adiabatic logic families largely depend upon itsa 12T SRAM cell is proposed to solve the problems caused by the reverse bias current. By avoiding the reverse bias current, the 12T SRAM shows a better HSNM, indicating that it is a promising candidate for ultra-low power applications. By adopting a write assist circuit, the proposed 12T SRAM cell has a better WSNM compared with those of the 7T SRAM cell and the combinational access SRAM cell and also has a lower write power. Additionally, the proposed 12T SRAM cell can effectively avoid the half-selected issue and improve circuit

performance by decoupling read. CLOCK RATE AND POWER can be reduced by using modified architectures as follows. The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have nearly negligible power consumption when sitting idle, in the region of a few micro-watts.

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